

DSP CIRCUITRY FOR SUPPORTING
MULTI-CHANNEL APPLICATIONS

Background of the Invention

[0001] This invention relates to digital signal
5 processing ("DSP") circuitry for use in programmable
logic devices, and more particularly to DSP circuitry
that can process multiple channels of data being
transmitted on the same carrier.

[0002] Programmable logic devices ("PLDs") are well
10 known for their ability to perform any of a wide range
of functions, depending on how they are programmed.
Programming may be done by storing data in control bits
on the PLD, by custom-configuring one or more layers of
the materials used to fabricate the PLD, or by any
15 other suitable means. Depending on the technology
employed, the programming may be volatile or non-
volatile, one-time-only or reprogrammable, etc.

[0003] In addition to the general-purpose circuitry
typically included in the architecture of a PLD, it is
20 also known to include various types of special-purpose
circuitry in such devices. Examples of such special-
purpose circuitry are blocks of memory, microprocessor
circuitry, DSP circuitry, etc. Advantages of using

special purpose circuitry is that they may be used to perform functions or process data independent of the programmable logic resources of the PLD, thus freeing those resources for other desired functions.

5 **[0004]** Consider, for example, existing DSP circuitry which can be used to perform common DSP task such as multiplication and filtering functions such as infinite impulse response filtering and finite impulse response filtering. Often times, it is desired that
10 conventional DSP circuitry perform these task on multiple channels of data being carried on a single carrier. Providing multiple channels on a single carrier is known and is sometimes referred to as time division multiplexing ("TDM"). In multi-channel or TDM
15 applications, each channel of data typically takes the form of a pulse modulation signal (e.g., pulse-amplitude modulation, pulse-width modulation, pulse-code modulation, etc.), which can be "interweaved" onto a signal carrier. This carrier signal is then
20 transmitted to some type of circuitry that "unweaves" the multiple channels of data without mixing any of the channels.

[0005] When conventional DSP circuitry independently processes multiple channels of data on a single
25 carrier, the channels often become mixed. That is, the data on one channel (e.g., channel 0) may be mixed with the data of another channel (e.g., channel 1), resulting in erroneous data processing. If multiple channels of data need to processed, using such
30 conventional DSP circuitry, the conventional DSP circuitry needs to interact with tap delay lines. As known in the art, tap delay lines include circuitry that registers multiple channels of data and enables

DSP circuitry to process each channel of data without experiencing cross-channel mixing.

[0006] Using this approach, however, requires that the tap delay lines be implemented using logic
5 resources. Such use of logic resources is inefficient at least because those logic resources are being devoted to a tap delay line when they could better utilized in providing other desired functions.

[0007] It would therefore be desirable to provide
10 DSP circuitry that can support multi-channel or time-division-multiplexing applications.

[0008] It would also be desirable to support multi-channel applications without requiring any utilization of logic resources.

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Summary of the Invention

[0009] It is therefore an object of the invention to provide improved DSP circuitry that supports multiple channel applications.

20 [0010] It is also an object of the invention to provide support multi-channel finite impulse response filter configurations.

[0011] These and other objects of the invention are provided by embedding an improved tap delay line
25 structure within DSP circuitry. This improved tap delay line structure enables the DSP circuitry to support multiple channel or TDM applications without having to rely on logic elements or other circuitry external to the DSP circuitry. Thus, by embedding the
30 circuitry of the invention within a DSP block, other circuitry such as logic elements, are free to be used for other desired operations.

[0012] The circuitry of the invention may be used in conjunction with a variety of DSP functions. For example, the circuitry of the invention can support multi-channel filter functions such as direct form I and II filter structures. The circuitry of the invention can be used in combination with hybrid multipliers implemented using both DSP circuitry and programmable logic circuitry.

[0013] Further features of the invention, its nature and various advantages, will be more apparent from the accompanying drawings and the following detailed description.

Brief Description of the Drawings

[0014] FIG. 1 is a simplified block diagram of an illustrative embodiment of a programmable logic device that can be constructed in accordance with the invention.

[0015] FIG. 2 is a simplified schematic diagram of DSP circuitry that can be constructed in accordance with the invention.

[0016] FIG. 3 shows a table that illustrates how circuitry of the invention does not mix channels as the data is processed in accordance with the invention.

[0017] FIG. 4 shows an illustrative use or configuration of a DSP block in accordance with the invention.

[0018] FIG. 5 shows a bar graph illustrating savings in logic resources that can be realized using circuitry in accordance with the invention.

[0019] FIG. 6 is a simplified schematic block diagram of an illustrative system employing a

programmable logic device in accordance with the invention.

Detailed Description

5 **[0020]** An illustrative programmable logic device ("PLD") integrated circuit 10 including digital signal processing ("DSP") blocks 20 in accordance with the invention is shown in FIG. 1. In addition to several DSP blocks 20-1 through 20-N, PLD 10 includes
10 programmable logic circuitry 30, general routing circuitry 40, and I/O circuitry 50. PLD 10 may also include one or more other types of circuitry 60 (e.g., blocks of memory circuitry, microprocessor circuitry, etc.). Programmable logic circuitry 30 is typically
15 programmable to perform any of a wide variety of logic tasks. General routing circuitry 40 is also typically programmable to at least a large degree and is provided to route signals to, from, and/or between other circuitries 20, 30, 50, and 60 (possibly also including
20 between various parts of those other circuitries, such as between various parts of programmable logic circuitry 30). I/O circuitry 50 is provided for making connections between PLD 10 and whatever external circuitry PLD 10 is used with. FIG. 1 also shows that
25 there may be various direct connections between adjacent ones of DSP blocks 20.

[0021] Typical of everything that is shown and described herein, FIG. 1 is intended to be illustrative and not limiting. For example, PLD 10 may also include
30 other circuitry and connections that are not shown in FIG. 1, or circuitries or connections shown in FIG. 1 may be omitted if desired. As an example of possible additions to what is shown in FIG. 1, some input

signals to PLD 10 may not pass through general routing circuitry 40. Certain high-speed signals (e.g., clock signals) may go directly to the circuit components (e.g., 20, 30, 60, etc.) that need those signals. As
5 another example of possible additions, PLD 10 may include so-called high-speed serial interface ("HSSI") circuitry that is dedicated to converting high-speed serial input signals to a form that is more readily dealt with by the remainder of the circuitry on PLD 10.
10 Such HSSI circuitry may directly receive data signals from external sources without those data signals passing through any general routing circuitry 40. As still another example of a possible addition to what is shown in FIG. 1, other connections between various
15 circuitries on the device may be provided if desired. For example, more direct connections (i.e., not via general routing circuitry 40) may be provided between DSP blocks 20 and programmable logic circuitry 30, between DSP blocks 20 and I/O circuitry 50, and/or
20 between DSP blocks 20 and other circuitry 60.

[0022] DSP circuitry 20 may be a medium through which PLD 10 processes certain types of digital signals to achieve suitable operating speeds without substantially impairing or using other resources of
25 PLD 10. DSP circuitry 20 may have capabilities that complement the capabilities of programmable logic circuitry 30. The complementary capabilities may sustain substantially concurrent use of substantially all of programmable logic circuitry 30 and DSP
30 circuitry 20. If desired, DSP circuitry 20 may operate without relying on distributed general routing circuitry 40 for performing internal DSP operations.

Thus, DSP circuitry 20 may operate as a high speed isolated DSP channel.

[0023] DSP circuitry 20 typically includes register circuitry, DSP utilization circuitry, interconnection circuitry, and other DSP circuitry. Register circuitry may be used to register data, which may be received from data sources (external to DSP circuitry 20) or from registers (within DSP circuitry 20). Data may be provided directly to DSP utilization circuitry by the data sources or register circuitry. DSP utilization circuitry may include, but not limited to, multiplier circuits, adder circuits, subtractor circuitry, and accumulator circuits. Interconnection circuitry may include connecting conductors and circuitry that interconnect the various circuitry (e.g., register circuitry and DSP utilization circuitry) of DSP circuitry 20. The interconnections may be programmable or dedicated. Interconnection circuitry can also include multiplexer circuits that can select which inputs signals are propagated to other circuitry.

[0024] The above-discussion of DSP circuitry 20 is illustrative of the content and organization of a single DSP circuit block. The various circuitry enables DSP circuitry 20 to perform a number of commonly used DSP operations such as infinite impulse response ("IIR") filters, direct form I finite impulse response ("FIR") filters, direct form II FIR filters, multiply accumulate operations, or any other suitable DSP operations.

[0025] A more detailed discussion of the structure of a PLD having integrated DSP circuitry is found in commonly-assigned Langhammer et al. U.S. Patent No.

6,538,470, which is hereby incorporated by reference herein in its entirety.

[0026] It will be understood that the foregoing description of a structure of a PLD having integrated
5 DSP circuitry is merely illustrative. The present invention may be practiced with respect to any other suitable PLD structure having integrated DSP circuitry. The present invention may, in fact, be practiced with a PLD coupled to external DSP circuitry. For purposes of
10 clarity and brevity, the present invention is described herein in terms of a PLD having integrated DSP circuitry.

[0027] The present invention is described herein primarily in terms of embedded tap delay line circuitry
15 that enables DSP circuitry 20 to support multi-channel or TDM applications. DSP circuitry 20 supports multi-channel or TDM applications by using a tap delay line circuit arrangement illustrated in FIG. 2. The circuit arrangement in FIG. 2 is an example of one specific
20 configuration and it is understood that like other features shown and described herein, FIG. 2 is intended to be illustrative and not limiting.

[0028] For convenience, the circuitry of the invention that enables DSP circuitry 20 to process
25 multiple channels of data is herein referred to as circuitry 100 (which is outlined by dashed lines in FIG. 2). Circuitry 100 may receive multiple channels of data, register the data to preserve channel integrity (i.e., prevent channels from mixing), and
30 provide data of the appropriate channel to DSP utilization circuitry 140.

[0029] Circuitry 100 may receive data being transmitted, for example, on general routing circuitry

40 or from any other suitable routing circuitry such as direct routing circuitry (not shown).

[0030] DSP utilization circuitry 140 includes circuitry (e.g., multiplier circuits, adder circuits, etc.) to operate on the data provided by circuitry 100. DSP utilization circuitry 140 is typically responsible for enabling DSP circuitry 20 to perform a desired DSP operation. For example, circuitry 140 may be constructed or be configurable to perform arithmetic operations of integers, real numbers, and imaginary numbers of various length (e.g., 9 bit, 18 bit, or 27 bit arithmetic). Circuitry 140 may enable DSP circuitry 20 to perform the operations needed to provide a FIR filter (e.g., a symmetrical, even order, or odd-order FIR filter). The complexity of DSP utilization circuitry 140 can range from simple circuitry such as multipliers to more complex circuitry such as hybrid multipliers. Examples of hybrid multipliers can be found, for example, in Esposito et al., U.S. Patent Application No. _____, filed, November 12, 2003, (Attorney Docket No. 174/257), the disclosure of which is incorporated in its entirety. Examples of other types of DSP utilization circuitry can found in Langhammer et al., U.S. Patent Application No. _____, filed October 3, 2003, (Attorney Docket No. 174/251), the disclosure of which is incorporated in its entirety. (FIG. 4 shows a schematic diagram of an embodiment of DSP utilization circuitry 140 that can be used to provide DSP circuitry 20 with FIR filtering operations.)

[0031] For brevity and clarity, DSP utilization circuitry 140, as shown in FIG. 2, includes multiplier circuits 142 and 144. Multiplier circuits 142 and 144

function as taps because these two circuits receive the data from circuitry 100. Thus, by convention, the circuitry arrangement shown in FIG. 2 is a two tap circuit.

5 [0032] As shown, circuitry 100 includes four columns of registers, two of which feed data to multiplier circuit 142 and the other two of which feed data to multiplier circuit 144. The columns, which are labeled as A, B, C, and D, each include an array of registers
10 arranged in serial. Each register may operate according the same clock signal (not shown, but each register shows a clock signal input). In accordance with this invention, the number of registers in each column may dictate the number of channels that can be
15 handled by DSP circuitry 20. Four registers are shown in the columns of circuitry 100, therefore DSP circuitry 20 can handle one to four channels. These registers are labeled according to the column in which they reside. As shown, column A includes registers
20 104a, 112a, 122a, and 132a, column B includes registers 104b, 112b, 122b, and 132b, and so forth for columns C and D. For convention, registers 104a-d may be referred to as leading registers and registers 132a-d may be referred to as trailing registers (the labeling
25 of which is based on the registers' relative positions in the column of registers).

 [0033] It is noted that the number of columns implemented in circuitry 100 is not limited to four. Any suitable number of columns may be included within
30 circuitry 100. For example, the number of columns may be a function of the physical size of DSP circuitry 20, the number of taps being implemented, or any other suitable factor.

[0034] It is noted that the number of registers included in circuitry 100 is not limited to the number of registers shown in FIG. 2. In order for the circuitry of the invention to provide multi-channel support, circuitry 100 should include at least 2 registers. Including at least two registers ensures that DSP circuitry 20 can correctly process at least two channels of data. Any suitable number of registers may be included each column.

10 [0035] Circuitry 100 also shows that each column has four multiplexer circuits. Each multiplexer circuit is associated with a register and is operative to selectively output one of at least two input signals to the associated registers. Selection of which inputs are transmitted to the associated register may be performed by control circuitry (not shown). The multiplier circuits, like the registers, are labeled according to the column in which they reside. As shown, column A includes multiplexer circuits 102a, 110a, 120a, and 130a, and column B includes multiplexer circuits 102b, 110b, 120b, and 130b, and so forth for columns C and D.

[0036] As will be explained in more detail below, multiplexer circuits 110a-d, 120a-d, and 130a-d may be part of bypass circuitry that can be used to selectively route data past certain ones of registers 104a-d, 112a-d, and 122a-d using bypass lead lines 160a-d. Use of tap delay lines 150, 152, 154, 156, 157, and 158 will also be discussed in more detail below. Note that the multiplexer circuits, tap delay lines, and bypass lead lines may collectively be considered as interconnection circuitry.

[0037] Beginning at the top of FIG. 2, circuitry 100 receives data X and Y from, for example, general routing circuitry. Data X and Y may carry N bits of data in parallel, where N represents the width of the bus. Data X and Y are shown being provided to two separate columns in circuitry 100. That is, data X is provided to multiplexer circuits 102a and 102c, whereas data Y is provided to multiplexer circuits 102b and 102d.

10 [0038] Multiplexer circuits 102a-d may also receive a second data input. This second data input may be provided by a data source external to circuitry 20 (e.g., another DSP block) or from a data source within DSP block 20 (e.g., the output of a register in a different column). For example, multiplexer circuits 102a and 102b may each receive a second data input from the output of registers residing in an adjacent DSP block via tap delay lines 150 and 152. Multiplexer circuit 102c may receive data from the output of register 132a via tap delay line 154 and multiplexer circuit 102d may receive data from the output of register 132b via tap delay line 156.

20 [0039] Multiplexers 102a-d, are controlled by one or more mode control signals (not shown) to select which input signal is to be passed to their respective registers. Thus, by way of example, multiplexer circuitry 102c can select either data X or the output of register 132b. If multiplexer circuitry 102c selects the data output of register 132b, then circuitry 100 utilizes tap delay line 154.

30 [0040] An advantage of this invention is that the tap delay lines are embedded within DSP circuitry 20, as opposed to DSP circuitry that utilizes tap delay

lines being implemented with logic resources external to the DSP circuitry. Tap delay lines of this invention route output signals of the trailing register (e.g., registers 132a-d) of one column to the input of a multiplexer circuit (e.g., multiplexer circuits 102a-d) in a different column. By way of example, the output of register 132a is provided to multiplexer circuit 102c and the output of register 132b is provided to multiplexer circuitry 102d. Note that in order to provide a finite impulse response system, the tap delay lines should provide the signals being provided to a tap (e.g., multiplier circuit 142) associated with one or more columns (e.g., a first group) to one or more adjacent columns (e.g., a second group) that is adjacent to the first group) that are associated with a different tap (e.g., multiplier circuit 144). By routing the trailing register outputs in this manner, DSP circuitry 20 can support multi-channel FIR applications.

20 **[0041]** To illustrate how the invention can be used in multi-channel or TDM applications consider FIGS. 2 and 3 in conjunction with each other. Assume that the multiplexer circuit mode controls are set to support four channels or a TDM factor of four. Although the bypass functionality of multiplexer circuits 110a-d, 120a-d, and 130a-d has not been discussed in detail, assume that these multiplexer circuits are not being instructed to bypass any registers. Further assume that multiplexer circuit 102c selectively provides the output of register 132a to register 104c and that multiplexer circuit 102d selectively provides the output of register 132b to register 104d. Further yet assume that that DSP utilization circuitry 140 is

configured to operate as a FIR filter. Based on the above-assumed configuration, the channel of the data being registered out of registers 132a-d is the same. That is, if registers 102a-b are providing channel 2 data to DSP utilization circuitry 140 (e.g., multiplier circuit 142), registers 102c-d are also providing channel 2 data to DSP utilization circuitry 140 (e.g., multiplier circuit 144).

[0042] FIG. 3 shows which channel (e.g., channel 0-3) is stored in registers 104a-d, 112a-d, 122a-d, and 132a-d for a given clock cycle. As shown, time steps t_0 - t_7 are placed on the y-axis and the registers are placed on the x-axis. Starting with time step t_0 , data on channel 0 is stored in registers 104a and 104b. Then at time step t_1 , the data on channel 0 is shifted to registers 112a and 112b, and data on channel 1 is shifted into registers 104a and 104b. As shown, the shifting of data continues each time step. At time step t_3 , all four channels are registered into circuitry 100. Then at time step t_4 , the channel 0 data of registers 132a and 132b is shifted to registers 104c and 104d by way of tap delay lines 154 and 156 and new channel 0 (denoted by 0') data is registered into registers 104a and 104b. Continuing down to time step t_7 , all sixteen registers of circuitry 100 have data stored therein.

[0043] Note the alignment of the channels as the data is stored in the registers. As shown, channel 0 data is stored in registers 132a-d, channel 1 data is stored in registers 122a-d, and so on. Thus at time step t_8 (not shown) the channel 0 data that was stored in registers 132a-d at time step t_7 is processed by DSP utilization circuitry 140. Accordingly, in each

successive time step, the same channel data is processed by DSP utilization circuitry 140 without the channels being mixed. For example, channel 0 data is not multiplied to channel 2 data.

5 **[0044]** Referring back to FIG. 2, note that the output of multiplexer circuits 102a-d, 110a-d, 120a-d, and 130a-d are fed directly to their respective registers. Further note bypass leads 160a-d, which route the outputs of multiplexer circuits 102a-d to
10 multiplexer circuits 110a-d, 120a-d, and 130a-d. The combination of bypass leads 160a-d and multiplexer circuits 110a-d, 120a-d, and 130a-d advantageously provides circuitry 100 with programmable flexibility in selecting the number of channels or the TDM factor
15 implemented by DSP circuitry 20. For example, if only two channels are needed, the data outputs of multiplexer circuits 102a-d may bypass registers 104a-d and 112a-d and be fed directly to registers 122a-d via bypass leads 160a-d. This way, two registers (e.g.,
20 registers 122a-d and 132a-d) are operative in each column to support both channels.

[0045] However, if data signals are not bypassing a register, the multiplexer circuits select the output of the preceding register and provide that output to that
25 multiplexer circuit's associated register. For example, if four channels are being processed by circuitry 100, multiplexer circuits 110a-d selectively route the output signal if registers 104a-d to registers 112a-d; multiplexer circuits 120a-d
30 selectively route the output signal if registers 110a-d to registers 122a-d; and multiplexer circuits 130a-d selectively route the output signal if registers 122a-d to registers 132a-d.

[0046] If desired, the bypass programmability of circuitry 100 may be omitted altogether. For example, if the number channels being used is known, circuitry 100 can be constructed with the requisite number of registers to support the desired number of channels. Doing this may eliminate the need for multiplexers 110a-d, 120a-d, and 130a-d.

[0047] Two or more DSP blocks 20 may be interconnected together to facilitate building of longer (i.e., more taps) FIR filters. The combination of DSP blocks 20 may be needed when the required number of columns exceeds the capacity of just one DSP block 20. For example, such expansion is apparent when multiplexor circuits 102a and 102b receive tap delay line inputs from trailing registers of an adjacent DSP block 20.

[0048] FIG. 4 shows multiplier/adder circuitry 140 that can be used with circuitry 100 of DSP block 20 to perform the operations needed to provide a two tap FIR filter operating on n-bit data samples, where n is the width of the data being processed by circuitry 100. Successive n-bit samples are shifted successively through registers 104a-d, 112a-d, 122a-d, and 132a-d in synchronism with a clock signal applied to all of those registers. In accordance with this invention, the data being shifted out of registers 132a-d correspond to the same channel, as illustrated above in connection with FIG. 3.

[0049] Continuing with FIG. 4, multiplier 420a is used to multiply the outputs of registers 132a and 132b. Multiplier 420b is used to multiply the outputs of registers 132c and 132d. Adder 430 is used to add

the outputs of multipliers 420a and 420b. Outputs RC are the FIR filter outputs.

[0050] One advantage of the circuitry of the invention is that it eliminates the need to use logic resources to support multi-channel or TDM applications. Thus, the circuitry of the invention frees up the logic elements that would have been used to support multi-channel or TDM applications for other suitable uses. FIG. 5 shows a graph that illustrates logic element savings that may be realized using the circuitry of the invention. As shown in FIG. 5, the logic element savings are shown as a function of tap size (e.g., 8, 16, 22, and 64 tap) and number of channels (e.g., two, three and four channels). It will be understood that the values shown in FIG. 5 are merely illustrative.

[0051] FIG. 6 illustrates a programmable logic device 10 of this invention in a data processing system 602. Data processing system 602 may include one or more of the following components: a processor 604; memory 606; I/O circuitry 608; and peripheral devices 610. These components are coupled together by a system bus 620 and are populated on a circuit board 630 (e.g., a printed circuit board), which is contained in an end-user system 640.

[0052] System 602 can be used in any of a wide variety of applications, such as computer networking, data networking, instrumentation, video processing, digital signal processing, or any other application where the advantage of using programmable or reprogrammable logic is desirable. Programmable logic device 10 can be used to perform a variety of different logic functions. For example, programmable logic device 10 can be configured as a processor or

controller that works in cooperation with processor 604. Programmable logic device 10 may also be used as an arbiter for arbitrating access to a shared resource in system 602. In yet another example, 5 programmable logic device 10 can be configured as an interface between processor 604 and one of the other components in system 602. It should be noted that system 602 is only exemplary, and that the true scope and spirit of the invention should be indicated by the 10 following claims.

[0053] Various technologies can be used to implement programmable logic devices 10 in accordance with this invention, as well as the various components of those devices (e.g., the logic connectors (such as the 15 depicted multiplexers) used to make connections throughout PLD 10, and the elements that control those logic connectors (the logic connectors being sometimes called "PLCs" and the control elements being called "FCEs")). For example, each PLC can be a relatively 20 simple programmable connector such as a switch or a plurality of switches for connecting any one of several inputs to an output. Alternatively, each PLC can be a somewhat more complex element that is capable of performing logic (e.g., by logically combining several 25 of its inputs) as well as making a connection. In the latter case, for example, each PLC can be product term logic, implementing functions such as AND, NAND, OR, or NOR. Examples of components suitable for implementing PLCs are EPROMs, EEPROMs, pass transistors, 30 transmission gates, antifuses, laser fuses, metal optional links, etc. As has been mentioned, the various components of PLCs can be controlled by various, programmable, function control elements

("FCEs"). (With certain PLC implementations (e.g., fuses and metal optional links) separate FCE devices are not required.) FCEs can also be implemented in any of several different ways. For example, FCEs can be

5 SRAMs, DRAMs, first-in first-out ("FIFO") memories, EPROMs, EEPROMs, function control registers (e.g., as in Wahlstrom U.S. patent 3,473,160), ferro-electric memories, fuses, antifuses, or the like. From the various examples mentioned above it will be seen that

10 this invention is applicable to both one-time-only programmable and reprogrammable devices.

[0054] It will be understood that the foregoing is only illustrative of the principles of the invention, and that various modifications can be made by those

15 skilled in the art without departing from the scope and spirit of the invention. For example, any number of DSP blocks 20 can be included in PLD 10. The particular operating modes shown and described herein are only illustrative, and many other operating modes

20 are also possible. It will also be understood that the circuitry of the invention could have been described as being arranged in rows as opposed to columns.